

Si9410DY

N-channel TrenchMOS™ logic level FET

Rev. 03 — 23 January 2004

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

2. Features

- Low on-state resistance
- Fast switching

3. Applications

- DC-to-DC converters
- DC motor control
- Lithium-ion battery applications
- Notebook PC
- Portable equipment applications.

4. Pinning information

Table 1: Pinning - SOT96-1 (SO8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	n/c	Top view MBK187	MBB076
2,3	source (s)		
4	gate (g)		
5,6,7,8	drain (d)		

SOT96-1 (SO8)



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
I_D	drain current (DC)	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$	-	7	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$	-	2.5	W
T_j	junction temperature		-	150	°C
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 7\text{ A}$	19	30	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 4\text{ A}$	23	40	mΩ
		$V_{GS} = 4.5\text{ V}$; $I_D = 3.5\text{ A}$	25	50	mΩ

6. Ordering information

Table 3: Ordering information

Type number	Package		
	Name	Description	Version
Si9410DY	SO8	Plastic small outline package; 8 leads	SOT96-1

7. Limiting values

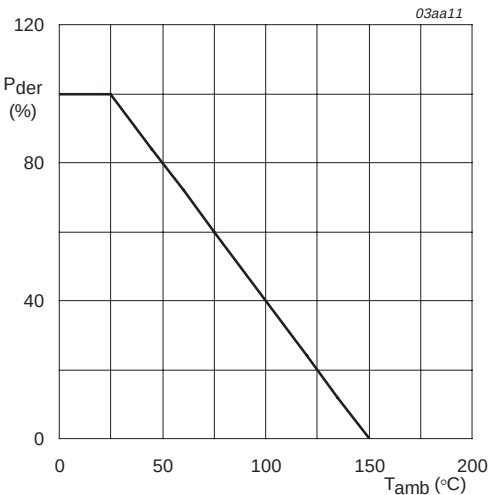
Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 2 and 3	-	7	A
		$T_{amb} = 70\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 2	-	5.8	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ μs}$; Figure 3	-	20.8	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 1	-	2.5	W
		$T_{amb} = 70\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 1	-	1.6	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C

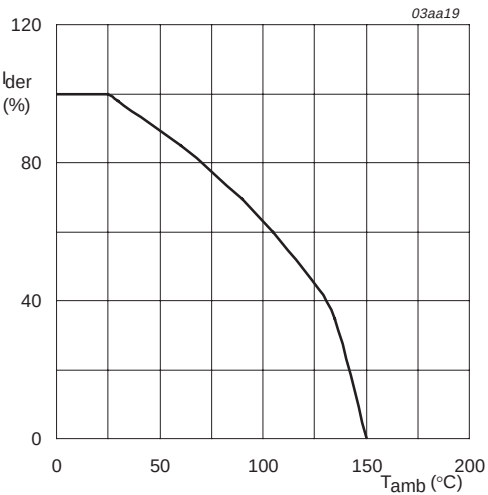
Source-drain diode

I_S	source (diode forward) current (DC)	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$	-	2.3	A
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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

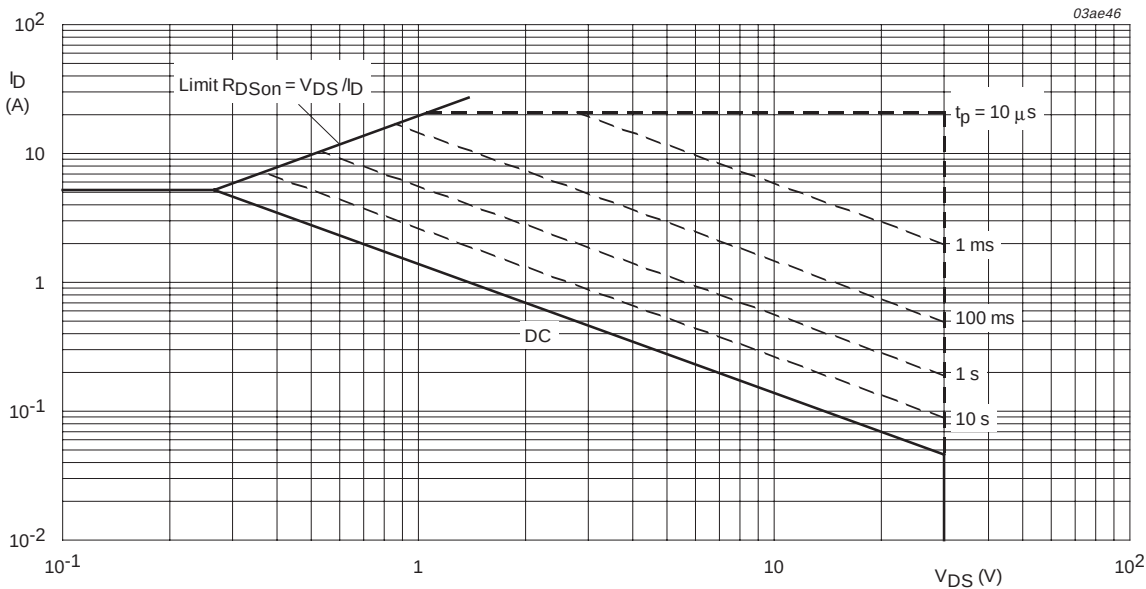
Fig 1. Normalized total power dissipation as a function of ambient temperature.



$$V_{GS} \geq 10 \text{ V}$$

$$I_D = \frac{I_{D(25^{\circ}C)}}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



$$T_{amb} = 25^{\circ}C; I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

8. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint, $t_p \leq 10$ s; Figure 4	-	-	50	K/W

8.1 Transient thermal impedance

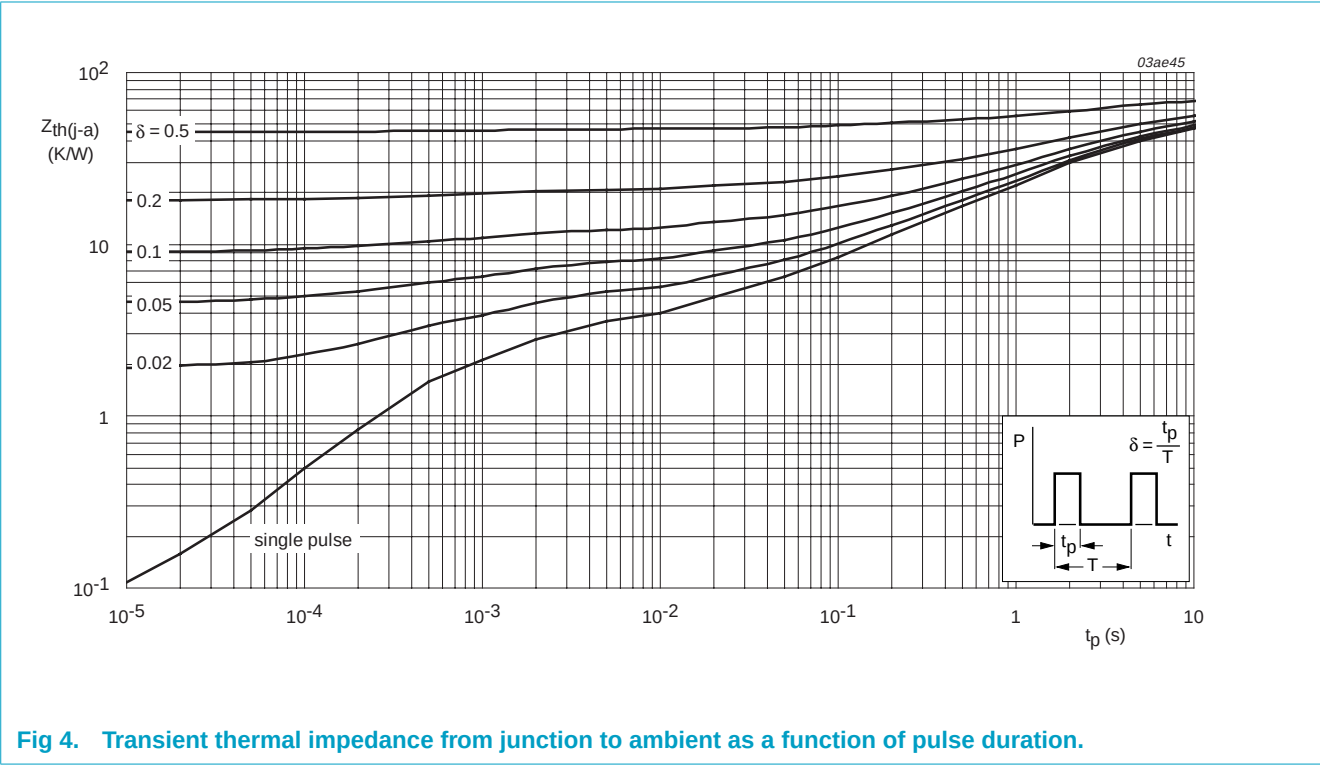


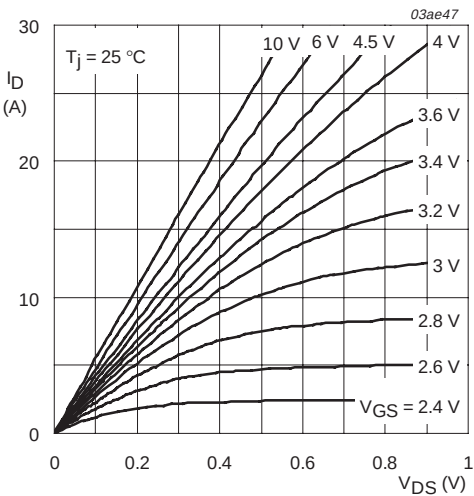
Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

9. Characteristics

Table 6: Characteristics

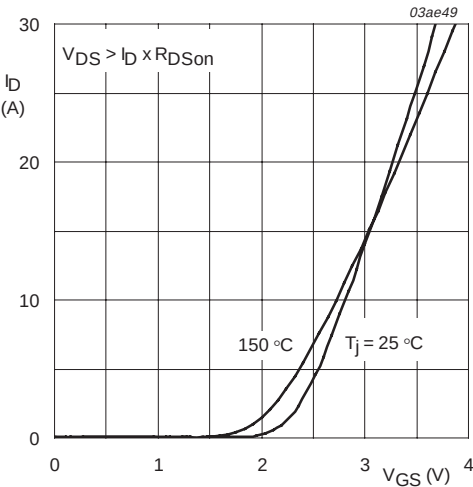
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{GS(th)}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; Figure 9	1	-	-	V
I _{DSS}	drain-source leakage current	V _{DS} = 24 V; V _{GS} = 0 V				
		T _J = 25 °C	-	-	2	μA
		T _J = 55 °C	-	-	25	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 7 A; Figure 7 and 8	-	19	30	mΩ
		V _{GS} = 5 V; I _D = 4 A; Figure 8	-	23	40	mΩ
		V _{GS} = 4.5 V; I _D = 3.5 A; Figure 7 and 8	-	25	50	mΩ
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 15 V; I _D = 7 A	-	15	-	S
Q _{g(tot)}	total gate charge	I _D = 7 A; V _{DS} = 15 V; V _{GS} = 10 V; Figure 13	-	14.6	50	nC
Q _{gs}	gate-source charge		-	2	-	nC
Q _{gd}	gate-drain (Miller) charge		-	3	-	nC
t _{d(on)}	turn-on delay time		V _{DD} = 25 V; R _D = 25 Ω; V _{GS} = 10 V; R _G = 6 Ω	-	5	30
t _r	rise time	-		6	60	ns
t _{d(off)}	turn-off delay time	-		21	150	ns
t _f	fall time	-		11	140	ns
Source-drain (reverse) diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 2 A; V _{GS} = 0 V; Figure 12	-	0.85	1.1	V
t _{rr}	reverse recovery time	I _S = 2 A; dI _S /dt = −100 A/μs; V _{GS} = 0 V	-	30	-	ns



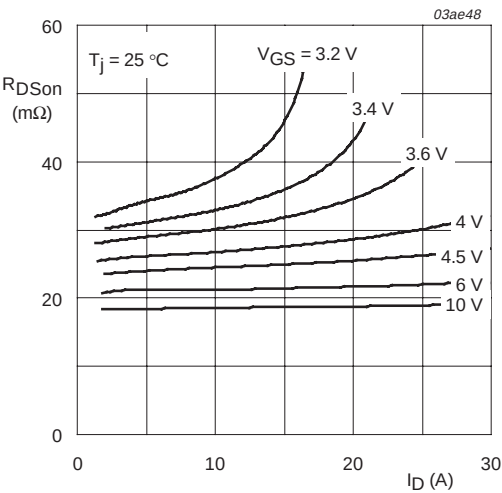
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



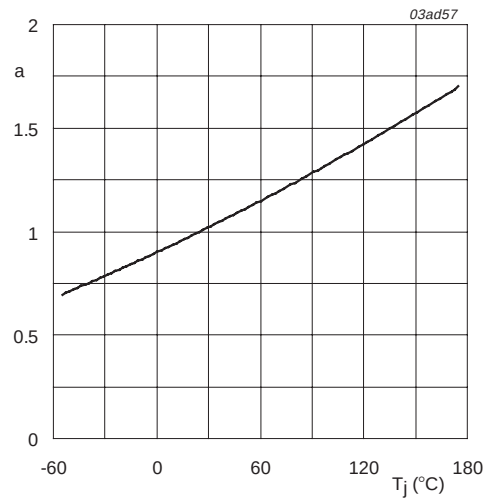
T_j = 25 °C and 150 °C; V_{DS} > I_D × R_{DSon}

Fig 6. Transfer characteristic: drain current as a function of gate-source voltage; typical values.



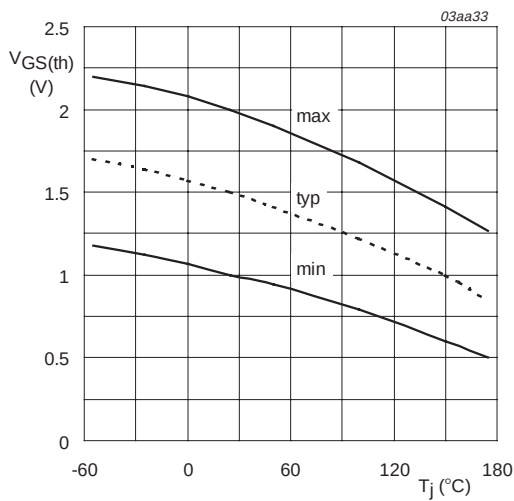
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



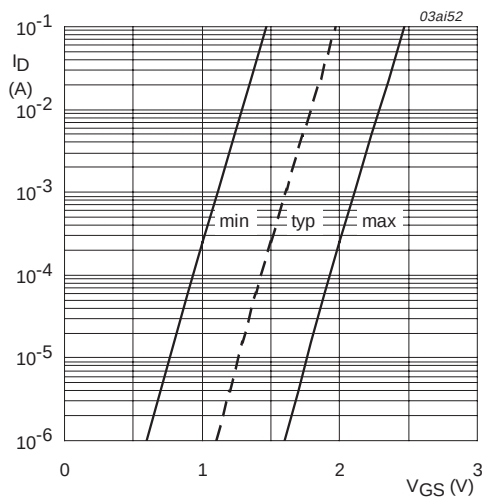
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



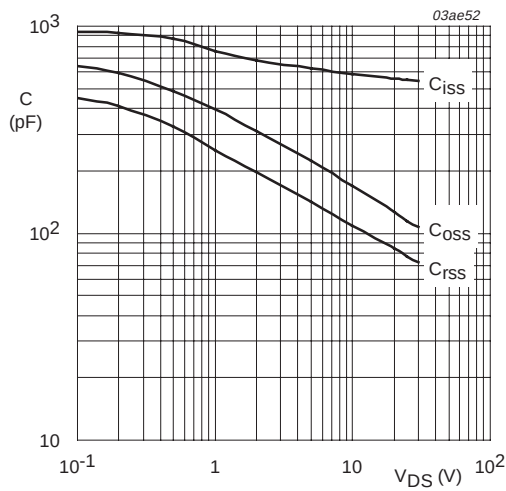
$I_D = 250 \mu A$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



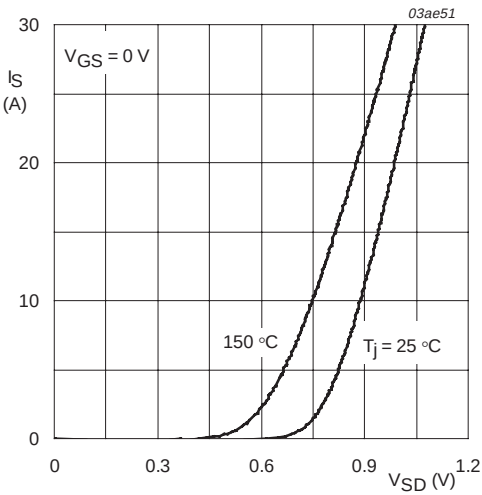
$T_j = 25 \text{ }^\circ\text{C}$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



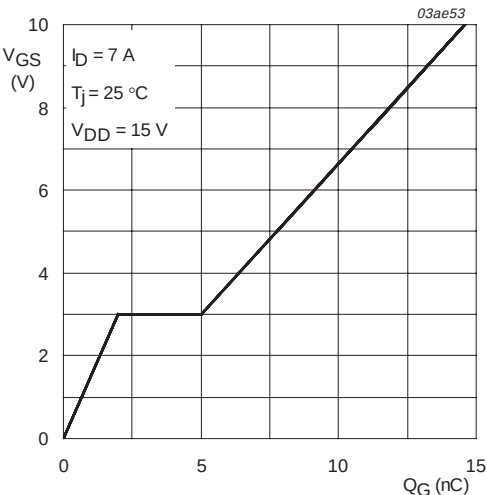
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 7\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

10. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

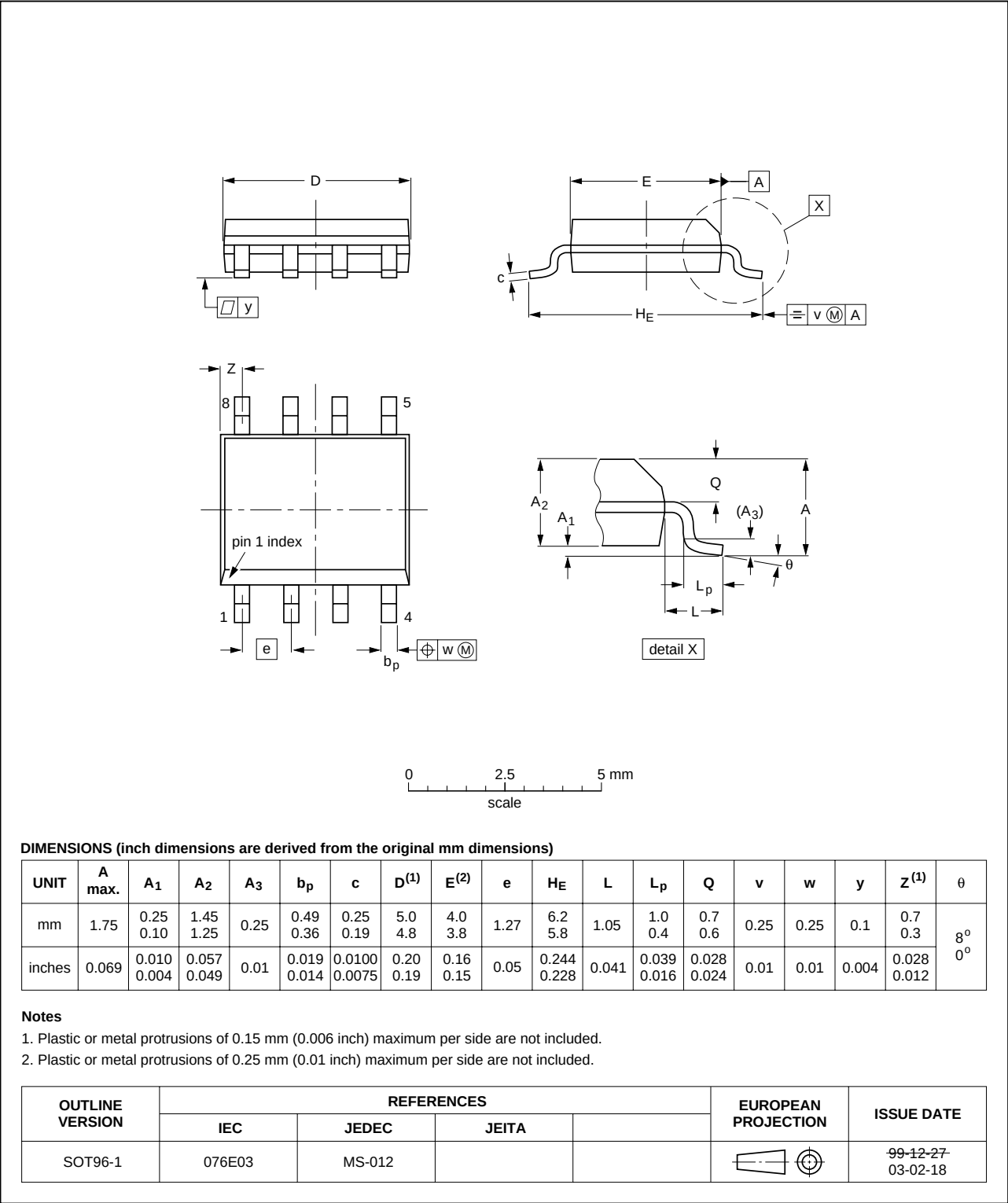


Fig 14. SOT96-1 (SO8).

11. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
03	20040123	HZG469	Product data (9397 750 12542) Modifications: • Updated to latest standards. • Section 7 “Limiting values” Figure 3 modified. • Section 8 “Thermal characteristics” Figure 4 modified. • Section 9 “Characteristics” R_{dson} modified. • Section 9 “Characteristics” $I_{\text{D(on)}}$ removed. • Section 9 “Characteristics” $Q_{\text{g(tot)}}$, Q_{gs} and Q_{gd} modified. • Section 9 “Characteristics” t_{don}, t_{r}, t_{doff} and t_{f} modified. • Section 9 “Characteristics” forward transfer characteristic graph removed. • Section 9 “Characteristics” t_{rr} removed. • Section 9 “Characteristics” Figure 5, 6, 7, 10, 11, 12 and 13 modified.
02	20010705	-	Product data (9397 750 08238) Modification: • Correction to I_{DM} condition.
01	20010515	-	Product data; initial version

12. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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